Claims

[c1] A method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches; and

creating a physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design,

wherein said creating of said physical design further comprises eliminating redundant latches, wherein redundant latches comprise latches which do not transition during the same clock cycle, do not relate to the same logical function, are in the same clock domain, and are within a given physical proximity of each other.

[c2] The method in claim 1, further comprising determining whether latches transition during the same clock cycle by running a simulation of an initial physical design and recording the latches that transition during each clock cycle.

[c3] The method in claim 2, wherein said process of determining whether latches transition during the same clock

cycle further comprises determining whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle.

[c4] The method in claim 1, wherein said process of eliminating redundant latches comprises replacing at least two redundant latches with a single latch.

[c5] The method in claim 1, wherein said process of eliminating redundant latches produces a revised physical design, and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected.

[c6] The method in claim 1, further comprising determining whether said latches relate to the same logical function by recording which latches are associated with each logical function in said logical design.

[c7] The method in claim 1, further comprising determining whether said latches are in the same clock domain by recording which latches are associated with each clock domain in said logical design.

[c8] A method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches;

creating an initial physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design;
preparing a database of transition times for said latches by running a simulation of an initial physical design and recording the clock cycle in which each latch transitions;
altering said initial physical design to eliminate redundant latches which do not transition during the same clock cycle.

[c9] The method in claim 8, wherein said altering of said initial physical design further considers whether latches relate to the same logical function, whether latches are in the same clock domain, and whether latches are within a given physical proximity of each other.

[c10] The method in claim 8, wherein said altering of said initial physical design further considers whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle.

[c11] The method in claim 8, wherein said altering of said initial physical design to eliminate redundant latches comprises replacing at least two redundant latches with a single latch.

[c12] The method in claim 8, wherein said altering of said initial physical design to eliminate redundant latches produces a revised physical design, and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected.

[c13] The method in claim 8, further comprising determining whether said latches relate to the same logical function by recording, in said database, which latches are associated with each logical function in said logical design.

[c14] The method in claim 8, further comprising adding selection logic connected to said latches, wherein said selection logic locks a non-active output to a known logical state when another output is active.

[c15] A method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches;

creating an initial physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design;

preparing a database of transition times for said latches by running a simulation of an initial physical design and recording the clock cycle in which each

latch transitions;

altering said initial physical design to eliminate redundant latches which do not transition during the same clock cycle, do not relate to the same logical function, are in the same clock domain, and are within a given physical proximity of each other.

[c16] The method in claim 15, wherein said altering of said initial physical design further considers whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle.

[c17] The method in claim 15, wherein said altering of said initial physical design to eliminate redundant latches comprises replacing at least two redundant latches with a single latch.

[c18] The method in claim 15, wherein said altering of said initial physical design to eliminate redundant latches produces a revised physical design, and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected.

[c19] The method in claim 15, further comprising determining whether said latches relate to the same logical function by recording, in said database, which latches are associ-

ated with each logical function in said logical design.

[c20] The method in claim 15, further comprising determining whether said latches are in the same clock domain by recording, in said database, which latches are associated with each clock domain in said logical design.

[c21] A method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches;

creating an initial physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design;

preparing a database of transition times for said latches by running a simulation of an initial physical design and recording the clock cycle in which each latch transitions;

determining whether said latches are in the same clock domain by recording, in said database, which latches are associated with each clock domain in said logical design;

altering said initial physical design to eliminate redundant latches which do not transition during the same clock cycle, do not relate to the same logical function, are in the same clock domain, and are within a given physical proximity of each other,

wherein said process of altering said initial physical design to eliminate redundant latches produces a revised

physical design, and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected.

[c22] The method in claim 21, wherein said altering of said initial physical design further considers whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle.

[c23] The method in claim 21, wherein said altering of said initial physical design to eliminate redundant latches comprises replacing at least two redundant latches with a single latch.

[c24] A method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches;

creating an initial physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design,

eliminating redundant latches from said initial physical design to create a revised physical design, and

adding selection logic connected to said latches in said revised physical design, wherein said selection logic includes outputs equal in number to the num-

ber of latches in said initial physical design and said selection logic locks a non-active output to a known logical state when a corresponding output is active.

[c25] The method in claim 24, wherein said adding of said selection logic comprises adding inverters and logical AND devices connected to said latches to make said outputs mutually exclusive.

[c26] The method in claim 24, wherein said adding of said selection logic permits one control signal to control a series of outputs similarly.

[c27] The method in claim 24, wherein redundant latches comprise latches which do not transition during the same clock cycle, do not relate to the same logical function, are in the same clock domain, and are within a given physical proximity of each other.

[c28] The method in claim 27, further comprising determining whether latches transition during the same clock cycle by running a simulation of an initial physical design and recording the latches that transition during each clock cycle.

[c29] The method in claim 28, wherein said process of determining whether latches transition during the same clock cycle further comprises determining whether an ade-

quate timing slack exists between transitions of latches that do not transition during the same clock cycle.

[c30] The method in claim 24, wherein said process of eliminating redundant latches comprises replacing at least two redundant latches with a single latch.

[c31] The method in claim 24, further comprising testing said revised physical design to determine whether said revised physical design performs as expected.

[c32] The method in claim 27, further comprising determining whether said latches relate to the same logical function by recording which latches are associated with each logical function in said logical design.

[c33] The method in claim 27, further comprising determining whether said latches are in the same clock domain by recording which latches are associated with each clock domain in said logical design.

[c34] A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches;

creating an initial physical design by positioning said

logic devices and said latches within said integrated circuit based on said logical design;
preparing a database of transition times for said latches by running a simulation of an initial physical design and recording the clock cycle in which each latch transitions;
altering said initial physical design to eliminate redundant latches which do not transition during the same clock cycle.

[c35] The program storage device in claim 34, wherein said altering of said initial physical design further considers whether latches relate to the same logical function, whether latches are in the same clock domain, and whether latches are within a given physical proximity of each other.

[c36] The program storage device in claim 34, wherein said altering of said initial physical design further considers whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle.

[c37] The program storage device in claim 34, wherein said altering of said initial physical design to eliminate redundant latches comprises replacing at least two redundant latches with a single latch.

[c38] The program storage device in claim 34, wherein said altering of said initial physical design to eliminate redundant latches produces a revised physical design, and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected.

[c39] The program storage device in claim 34, wherein said method further comprises determining whether said latches relate to the same logical function by recording, in said database, which latches are associated with each logical function in said logical design.

[c40] The program storage device in claim 34, wherein said method further comprises determining whether said latches are in the same clock domain by recording, in said database, which latches are associated with each clock domain in said logical design.